WE CLAIM:

1. A method of concurrently generating a plurality of clock signals derived from a reference signal, said method comprising:

receiving said reference signal;

producing a plurality of signals each having a frequency and a different phase;

dividing said frequency of each of said produced signals concurrently in accordance with programmable selections of frequency divisors to produce output signals each having a frequency and phase; and

multiplexing said output signals in accordance with programmable selections such that each clock signal is usable as an off-chip clock signal, an on-chip clock signal, or both.

2. The method of claim 1 wherein said frequency of each of said output signals is different than or the same as one or more of the other of said output signals.

3. The method of claim 1 wherein said multiplexing comprises programmably coupling one of said output signals to an output pin for use as an off-chip clock signal.

4. The method of claim 1 wherein said multiplexing comprises programmably coupling one of said output signals to a global clock network for use as an on-chip global clock signal, said global clock network being on the same integrated circuit chip on which said producing and said dividing are performed.

5. The method of claim 1 wherein said multiplexing comprises programmably coupling one of said output signals to a clock network for use as an on-chip local clock signal, said clock network coupled to only a portion of circuits on an integrated circuit chip, said integrated circuit chip being the same on which said producing and said dividing are performed.

6. The method of claim 1 further comprising:

receiving a plurality of input signals;

synchronizing said plurality of input signals with an enable signal; and

selecting one of said plurality of input signals to be said reference signal.

7. The method of claim 5 wherein said receiving comprises:

generating one of said plurality of input signals on an integrated circuit chip on which said producing and said dividing are performed; and

receiving from another integrated circuit chip via an input pin another one of said plurality of input signals.

8. A method of providing a plurality of clock signals concurrently, said method comprising:

programming a first divisor into a first frequency divider that receives a reference signal;

programming a plurality of divisors into a respective plurality of frequency dividers that receive

substantially concurrently a signal processed by said first frequency divider; and

programming at least one multiplexer to couple one of a plurality of output signals received from said plurality of frequency dividers to any one of an integrated circuit output pin, a global clock network, or a local clock network.

9. The method of claim 8 further comprising after said programming a plurality of divisors:

programming the output of one of said plurality of frequency dividers to be fed into another one of said plurality of frequency dividers.

10. The method of claim 9 further comprising repeating said programming the output at least once.

11. A method of converting an input clock signal to a plurality of output clock signals, said method comprising:

modifying said input clock signal having an input frequency to produce a first signal having a first frequency;

phase-shifting said first signal to produce a plurality of second signals each having a phase and said first frequency, each of said second signals having a phase different than the phase of the others of said second signals;

modifying each of said second signals substantially concurrently to produce an output signal having a phase and an output frequency, each of said output signals having an individually selectable output frequency; and

selectably coupling any one of said output signals to an integrated circuit chip output pin;

selectably coupling any one of said output signals to a global clock network, said global clock network providing clock signals to all clockable circuits on an integrated circuit chip; and

selectably coupling any one of said output signals to at least one local clock network, said local clock network providing clock signals to only a portion of clockable circuits on said integrated circuit chip.

12. A method of providing multiple clock signals based on a reference signal, said method comprising:

generating a first plurality of clock signals in response to receiving said reference signal; each of said plurality of clock signals having a different phase;

generating concurrently a second plurality of clock signals each having a phase and a selectable frequency; and

making each of said second plurality of clock signals available for a same plurality of clocking applications.

13. The method of claim 12 wherein said clocking applications include off-chip clocking, on-chip global clocking, on-chip local clocking, frequency synthesizing, and zero delay buffering.

14. A circuit on a programmable logic device operative to output a plurality of clock signals having programmable phases and frequencies, said circuit comprising:

first frequency-divider circuitry operative to receive an input signal;

phase/frequency detector circuitry coupled to receive the output of said frequency divider and having a second input;

a voltage-controlled oscillator (VCO) coupled to receive the output of said phase/frequency detector circuitry and operative to output a plurality of signals each having a different phase;

feedback frequency-divider circuitry coupled to receive said plurality of VCO output signals and operative to output a frequency-divided signal to said second input of said phase/frequency detector;

first multiplexing circuitry coupled to receive said plurality of VCO output signals and operative to output a plurality of signals selected from said plurality of VCO output signals;

a plurality of frequency dividers each coupled to said multiplexing circuit to receive one of said output signals from said first multiplexing circuitry and operative to output a frequency-divided signal; and

second multiplexing circuitry coupled to receive each of said frequency-divided signals from said plurality of frequency dividers, said second multiplexing circuitry operative to programmably output each received frequency-divided signal to any one of a plurality of signal conductors coupled to said second multiplexing circuitry.

15. The circuit of claim 14 wherein said plurality of signal conductors are coupled to clock output pins, a global clock network, and at least one local clock network.

16. The circuit of claim 14 further comprising third multiplexer circuitry coupled to receive a plurality of input signals and operative to programmably output one of said signals to said first frequency-divider circuitry.

17. The circuit of claim 16 wherein said third multiplexer circuitry comprises a synchronization circuit coupled to receive an enable signal and a selectable two of said plurality of input signals, said synchronization circuit comprising two latches clocked by said enable signal, each latch coupled to receive a respective one of said selectable two signals and operative to output a synchronized signal.

18. The circuit of claim 17 further comprising switchover circuitry coupled to receive said two synchronized signals from said two latches and operative to automatically output the other of said two synchronized signals should one of said two synchronized signals not be received.

19. The circuit of claim 14 wherein said feedback frequency-divider circuitry comprises a multiplexer and a programmable frequency-divider circuit, said multiplexer coupled to receive said plurality of VCO output signals and operative to output one of said VCO output signals to said frequency-divider circuit, said frequency-divider circuit operative to output a frequency-divided signal to said second input of said phase/frequency detector.

20. The circuit of claim 14 wherein said circuit is a low voltage differential signaling (LVDS) phase-locked loop circuit.

21. The circuit of claim 14 wherein said circuit is a general purpose phase-locked loop circuit.

22. An integrated circuit chip comprising the circuit of claim 14.

23. A programmable logic device comprising the circuit of claim 14.

24. A printed circuit board comprising the circuit of claim 14 mounted on said printed circuit board.

25. The printed circuit board of claim 24 further comprising a memory mounted on said printed circuit board.

26. The printed circuit board of claim 24 further comprising processing circuitry mounted on said printed circuit board.

27. A system comprising:

a processor;

a memory coupled to said processor; and

the circuit of claim 14 coupled to at least one of said processor and said memory.

28. A digital processing system comprising:

a processor;

a memory;

a programmable logic device comprising the circuit of claim 13;

input/output circuitry; and

a system bus coupling said processor, said memory, said programmable logic device, and said input/output circuitry.

29. A phase-locked loop circuit comprising:

means for phase-shifting a received signal to produce a plurality of phase-shifted signals, each phase-shifted signal having a frequency and being shifted by a different amount;

means for modifying the frequency of at least a subplurality of said phase-shifted signals; and

means for selectively applying each of said frequency-modified signals to any one of several clocking networks.

30. The phase-locked loop circuit of claim 29 wherein said clocking networks include an off-chip network and an on-chip network, said chip comprising the phase-locked loop circuit of claim 29.